

REMARKS

Reconsideration and allowance are respectfully requested in view of the following remarks.

Claims 1-2, 4-5, 6-10, 12-13, 15-20 and 22-23 were rejected under 35 U.S.C. 102(b) as being anticipated by Micheloni. Applicants respectfully traverse.

Turning first to claim 1, Applicants have amended claim 1 to recite that the system includes, “in parallel with each program load circuit, a current sinking conduction-to-ground path that includes an enabling controlled active element” (emphasis added). The Examiner has asserted that Micheloni teaches a conduction to ground path through capacitor Cpar2 which is enabled by transistor YN.

In amending claim 1, Applicants emphasize that the conduction to ground path is “current sinking.” Such is not the case with capacitor Cpar2 in Micheloni. The path cited by the Examiner is not a true path of current to ground since it is well known to one skilled in the art that it is not possible to drive a constant current through a path that includes a series connected capacitor. The path through capacitor Cpar2 in Micheloni thus is not, and cannot, be a “current sinking conduction-to-ground path” (emphasis added).

The inability and failure of the path through capacitor Cpar2 in Micheloni to be current sinking is further confirmed from a review of Micheloni’s teachings. Micheloni states that capacitor Cpar2 is a parasitic capacitance associated with the hierarchic decoder of the circuit (col. 7, lines 18-21). This capacitance functions, not to sink current as claimed, but rather as a source of current that is supplied to charge the bit line (col. 8, lines 52-56).

In amending claim 1, Applicants further emphasize that the conduction-to-ground path “includes an enabling controlled active element” (emphasis added). This conduction-to-ground path furthermore is claimed to be “in parallel with each program load circuit.” Such a circuit configuration is not shown by Micheloni. While the capacitor Cpar2 is shown connected in parallel with the program load circuit of transistors YN and YO, that parallel path consists solely of the capacitor Cpar2 itself. That parallel path does not include, as is claimed by Applicants, “an enabling controlled active element” (emphasis added). Instead the transistors YN and YO are actually a part of the program load circuit, thus precluding that structure from meeting the claimed “in parallel with each program load circuit” limitation.

In view of the foregoing, Applicants respectfully submit that claim 1 is neither anticipated nor obvious in view of the cited Micheloni reference.

With respect to dependent claims 4 and 5, Applicants claim that the path is a redundant/dummy current path. As discussed above, the path through capacitor Cpar2 in Micheloni is a current source used to charge the bit lines. There is no teaching or suggestion for this path to function as a redundant or dummy current path. Rather, the path through capacitor Cpar2 is actually associated with the hierachic decoder of the circuit. There is no disclosure or teaching for such a decoder to be a part of any redundant or dummy circuitry. Claims 4 and 5 accordingly are not anticipated by Micheloni.

Turning next to claim 6, Applicants have amended the claim to recite “a selectively actuated current sinking conduction to ground path coupled to the bit line” (emphasis added). The Examiner has asserted that Micheloni teaches a conduction to ground path through capacitor

Cpar2 which is enabled by transistors YO and YN. Applicants however claim that the conduction to ground path is “current sinking.” Such is not the case with capacitor Cpar2 in Micheloni. The path cited by the Examiner is not a true path of current to ground since it is well known to one skilled in the art that it is not possible to drive a constant current through a path that includes a series connected capacitor. The path through capacitor Cpar2 in Micheloni thus is not, and cannot, be a “current sinking conduction to ground path” (emphasis added).

The inability and failure of the path through capacitor Cpar2 in Micheloni to be current sinking is further confirmed from a review of Micheloni’s teachings. Micheloni states that capacitor Cpar2 is a parasitic capacitance associated with the hierarchic decoder of the circuit (col. 7, lines 18-21). This capacitance functions, not to sink current as claimed, but rather as a source of current that is supplied to the bit line (col. 8, lines 52-56).

In view of the foregoing, Applicants respectfully submit that claim 6 is neither anticipated nor obvious in view of the cited Micheloni reference.

In claim 12, Applicants claim “a column programming circuit coupled between a programming voltage source and each bit line and activated in response to a first control signal.” The Examiner has asserted that this limitation is met by Micheloni with respect to the HWSWx circuits where VPD is the programming voltage source. The Micheloni circuitry at issue must further include transistors PL, YM, YN and YO because the claim recites that the “column programming circuit [is] coupled between a programming voltage source and each bit line.” Applicants further claim “a bypass path circuit for each bit line and **coupled between the programming voltage source and ground** and activated in response to a second control signal”

(emphasis added). The Examiner asserts that the claimed bypass path is met by the source/drain path through transistor YN, node XY and transistor Cpar2. It is clear, however, that this path asserted by the Examiner to be the claimed bypass path IS NOT coupled between VPD and ground as is specifically recited by claim 12. Rather, this path is coupled between the bit line at node VD and ground. Thus, Micheloni does not anticipate the claimed invention, and claim 12 is in condition for favorable action and allowance.

With respect to claim 16, Applicants further claim that the bypass path circuit, which is coupled between the programming voltage source and ground, comprises a pass transistor. The Examiner asserts that transistor YN in Micheloni meets this limitation. Applicants respectfully disagree. The transistor YN is coupled between the bit line at node VD and ground (through the capacitor). There is no teaching or suggestion for transistor YN being coupled between the programming voltage source and ground as claimed. Thus, claim 16 is not anticipated by Micheloni.

In claim 17, Applicants claim “a current sinking conduction-to-ground path for each matrix column, each path being **enabled when its associated matrix column is not selected** during the programming operation” (emphasis added). First, Applicants have amended the claim to recite “a current sinking conduction-to-ground path.” For at least the reasons recited above with respect to claim 6, this claim is not anticipated by or obvious in view of the Micheloni reference.

Second, Applicants claim that this path is “enabled when its associated matrix column is not selected.” Such an operation is clearly not taught by Micheloni. As discussed above, the

capacitor Cpar2 is a parasitic capacitance associated with the hierarchic decoder of the circuit (col. 7, lines 18-21). This capacitance provides a source of current that is supplied to the bit line when the bit line is selected (col. 8, lines 52-56). Thus, the path through capacitor Cpar2 cited by the Examiner is not “enabled when its associated matrix column is not selected,” as claimed, but RATHER IS ENABLED when its associated matrix column IS SELECTED. This is the opposite operation from that claimed by Applicants.

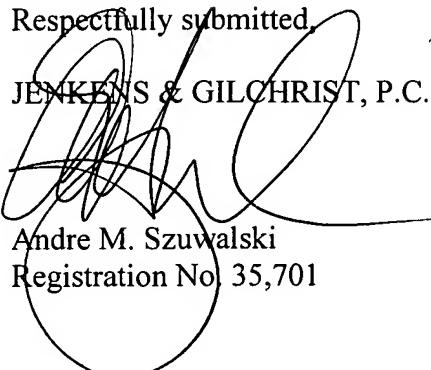
In view of the foregoing, Applicants respectfully submit that claim 17 is neither anticipated nor obvious in view of the cited Micheloni reference.

With respect to claims 22 and 23, Applicants respectfully submit that these claims are not anticipated by Micheloni. The path through capacitor Cpar2 in Micheloni is a current source used to charge the bit lines. There is no teaching or suggestion for this path to function as a redundant or dummy current path. Rather, the path through capacitor Cpar2 is actually associated with the hierarchic decoder of the circuit. There is no disclosure or teaching for such a decoder to be a part of any redundant or dummy circuitry.

CUSTOMER NO. 23932

PATENT APPLICATION
Docket No. 61181-13USPX

In view of the above, it is believed that this application is in condition for allowance, and such a Notice is respectfully requested.

Respectfully submitted,

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